What is claimed is:

1. A method for forming a lower electrode of a capacitor in a semiconductor device, including the steps of:

forming a first layer of the lower electrode over a substrate, the first layer comprising a material that serves as a barrier against the diffusion of impurities from the substrate;

forming a second layer of the lower electrode over the first layer, the second layer comprising a material that is easy to pattern; and

forming a third layer of the lower electrode over the second layer, the third layer comprising a material having low leakage current properties.

2. A method for forming the lower electrode of a capacitor according to claim 1, wherein the first layer of the lower electrode comprises TiN.

3. A method for forming the lower electrode of a capacitor according to claim 1, wherein the second layer of the lower electrode comprises RuO_2.

4. A method for forming the lower electrode of a capacitor according to claim 1, wherein the third layer of the lower electrode comprises Pt.

5. A method for forming the lower electrode of a capacitor according to claim 1, wherein the lower electrode is in contact with a dielectric layer.

6. A method for forming the lower electrode of a capacitor according to claim 5, wherein the dielectric layer is a high-dielectric layer comprising a material from the group consisting of $SrTiO_3$ and $(Ba_xSr_{1-x})TiO_3$.

7. A method for forming the lower electrode of a capacitor according to claim 5, wherein the dielectric layer is deposited by a CVD method.

8. A method for manufacturing a capacitor including the steps of:

forming an insulating film on a semiconductor substrate;

forming a contact hole in the insulating film;

forming a polysilicon plug in the contact hole;

depositing a first layer over the contact hole, the first layer comprising a material that serves as a barrier against the diffusion of impurities from the semiconductor substrate;

depositing a second layer over the first layer, the second layer comprising a material that is easy to pattern;

forming a hard mask pattern over the second layer;

sequentially patterning the first and second layers;

depositing a third layer over the patterned first and second, the third layer comprising a material having low leakage current properties;

forming a dielectric layer on the third layer; and

forming an upper electrode on the dielectric layer.

9. A method for manufacturing a capacitor according to claim 8, wherein the first layer comprises TiN.

10. A method for manufacturing a capacitor according to claim 8, wherein the second layer comprises RuO_2.

11. A method for manufacturing a capacitor according to claim 8, wherein the third layer comprises Pt.

12. A method for manufacturing a capacitor according to claim 8, wherein the steps of depositing the first and second layers are carried out through the use of a reactive DC sputtering process.

13. A method for manufacturing a capacitor according to claim 8, wherein the hard mask pattern comprises silicon-on-glass (SOG).

14. A method for manufacturing a capacitor according to claim 8, wherein the patterning step is carried out through the use of a reactive ion etching method.

15. A method for manufacturing a capacitor according to claim 8, wherein the dielectric layer comprises a high-dielectric film.

16. A method for manufacturing a capacitor according to claim 8, wherein the dielectric layer comprises a material from the group consisting of $SrTiO_3$ and $(Ba_xSr_{1-x})TiO_3$.

17. A method for manufacturing a capacitor according to claim 8, wherein the step of depositing the third layer is performed by using a sputter method so that the third layer deposited over the top and sides of the first and second layers will have a variable thickness.

18. A method for manufacturing a capacitor according to claim 17, wherein said third layer deposited over the top of the first and second layers is approximately 200Å thick.

19. A method for manufacturing a capacitor according to claim 18, further comprising a step of etching back the third layer to uniformly control the thickness of the third layer.

20. A method for manufacturing a capacitor according to claim 19, wherein the third layer is overetched together with a portion of an interlayer insulating film formed below the third layer, to achieve complete isolation between node patterns during the step of etching back the third layer.

21. A method for manufacturing a high dielectric capacitor according to claim 19, wherein step of etching back the third layer is controlled to maintain the thickness of the third layer on the top and sides of the node pattern at approximately 60Å.

22. A method for manufacturing a capacitor according to claim 8, further comprising a step of etching back the third layer to uniformly control the thickness of the third layer.

23. A method for manufacturing a high dielectric capacitor according to claim 22, wherein the third layer is overetched together with a portion of an interlayer insulating film formed below the third layer, to achieve complete isolation between node patterns during the step of etching back the third layer.

24. A method for manufacturing a high dielectric capacitor according to claim 22, wherein step of etching back the third layer is controlled to maintain the thickness of the third layer on the top and sides of the node pattern at approximately 60Å.

25. A lower electrode of a capacitor in a semiconductor device, comprising:

a first layer comprising a material that serves as a barrier against the diffusion of impurities from a lower substrate;

a second layer formed over the first layer, the second layer comprising a material that is easy to pattern; and

a third layer formed over the second layer, the third layer comprising a material having low leakage current properties.

26. A lower electrode of a capacitor according to claim 25, wherein the first layer comprises TiN.

27. A lower electrode of a capacitor according to claim 25, wherein the second layer comprises RuO_2.

28. A lower electrode of a capacitor according to claim 25, wherein the third layer comprises Pt.